Serial No. 09/943,078
Docket No. MIO 0083 PA

Amendments to the Claims

The following listing of claims will replace all prior versions, and listings, of claims in the present application:

Please cancel claims 1, 8, 10 and 17-28 and amend claims 2, 5-7, 9, 11, 14-16, 39 and 45-47 as follows:

1. (canceled)

C2

2. (currently amended) A method of fabricating a semiconductor device according to claim [[1]]7, further comprising forming an isolation trench in said base substrate before said first dielectric layer is formed.

3. (original) A method of fabricating a semiconductor device according to claim 2, wherein at least a portion of said damascene trench at least partially overlies said isolation trench.

4. (previously presented) A method of fabricating a semiconductor device according to claim 2, wherein said isolation trench formation comprises:

etching into said base substrate defining an isolation trench opening in said base substrate; and

filling said isolation trench opening with a dielectric material.

5. (currently amended) A method of fabricating a semiconductor device according to claim [[1]]7, wherein said first dielectric layer formation comprises depositing a conformal inter-layer dielectric material over said base substrate.

6. (currently amended) A method of fabricating a semiconductor device according to claim [[1]]7, wherein said damascene trench formation comprises:

forming a patterned mask over said first dielectric layer;

etching through said first diel ctric layer to said base substrate in areas defined by said patterned mask; and[[,]]

stripping said patterned mask from said first dielectric layer.

7. (currently amended) A method of fabricating a semiconductor device ~~according to claim 1, further~~ comprising:

C2 Cont.

forming a first dielectric layer over a base substrate;

forming a damascene trench in said first dielectric layer, said damascene trench having a gate area and a local interconnect area;

forming a gate oxide layer on said base substrate within said gate area of said damascene trench;

depositing a conductive layer over said base substrate such that said damascene trench is filled with a conductive material;

planarizing said device to define a damascene structure including a damascene gate structure and a damascene local interconnect structure electrically coupled by said conductive material within said damascene trench, wherein said damascene local interconnect structure forms a connection to said base substrate;

removing said first dielectric layer; and

providing at least one implant within said base substrate through said damascene trench.

8. (canceled)

9. (currently amended) A method of fabricating a semiconductor device ~~according to claim 8, further~~ comprising:

forming a first dielectric layer over a base substrate;

forming a damascene trench in said first dielectric layer, said damascene trench having a gate area and a local interconnect area;

forming a gate oxide layer on said base substrate within said gate area of said damascene trench, wherein said gat oxid layer formation comprises

growing an oxide layer on said base substrate,

forming a patterned mask over said semiconductor device, said pattern arranged to expose at least a portion of said oxide layer within said local interconnect area,

etching away the exposed portion of said oxide layer, and

stripping said patterned mask from said semiconductor device;

depositing a conductive layer over said base substrate such that said damascene trench is filled with a conductive material;

planarizing said device to define a damascene structure including a damascene gate structure and a damascene local interconnect structure electrically coupled by said conductive material within said damascene trench, wherein said damascene local interconnect structure forms a connection to said base substrate;

C2 Cont.

removing said first dielectric layer; and

providing a contact implant within said base substrate through said damascene trench prior to stripping said patterned mask.

10. (canceled)

11. (currently amended) A method of fabricating a semiconductor device ~~according to claim 10, further~~ comprising:

forming a first dielectric layer over a base substrate;

forming a damascene trench in said first dielectric layer, said damascene trench having a gate area and a local interconnect area;

forming a gate oxide layer on said base substrate within said gate area of said damascene trench;

depositing a conductive layer over said base substrate such that said damascene trench is filled with a conductive material, wherein said conductive material comprises a polysilicon material;

planarizing said device to define a damascene structure including a damascene gate structure and a damascene local interconnect structure electrically coupled by said conductive material within said damascene trench, wherein said damascene local interconnect structure forms a connection to said base substrat ;

removing said first diel ctric layer; and

forming a silicide layer over said polysilicon material within said gate area of said damascene trench.

12-13. (cancelled)

14. (currently amended) A method of fabricating a semiconductor device ~~according to claim 1, further~~ comprising:

C2 Cont.

forming a first dielectric layer over a base substrate;

forming a damascene trench in said first dielectric layer, said damascene trench having a gate area and a local interconnect area;

forming a gate oxide layer on said base substrate within said gate area of said damascene trench;

depositing a conductive layer over said base substrate such that said damascene trench is filled with a conductive material;

planarizing said device to define a damascene structure including a damascene gate structure and a damascene local interconnect structure electrically coupled by said conductive material within said damascene trench, wherein said damascene local interconnect structure forms a connection to said base substrate;

removing said first dielectric layer; and

forming lightly doped drain regions in said base substrate after removing said first dielectric layer, said lightly doped drain regions formed within said base substrate adjacent to said damascene gate structure and said damascene local interconnect structure.

15. (currently amended) A method of fabricating a semiconductor device according to claim 14, further comprising forming spacers against the vertical walls of said damascene gate structure and said damascene local interconnect structure.

16. (currently amended) A method of fabricating a semiconductor device ~~according to claim 1, further~~ comprising:

forming a first dielectric layer over a base substrate;

forming a damascene trench in said first dielectric layer, said damascene trench having a gate area and a local interconnect area;

forming a gate oxide layer on said base substrate within said gate area of said damascene trench;

depositing a conductive layer over said base substrate such that said damascene trench is filled with a conductive material;

planarizing said device to define a damascene structure including a damascene gate structure and a damascene local interconnect structure electrically coupled by said conductive material within said damascene trench, wherein said damascene local interconnect structure forms a connection to said base substrate;

C2 cont.

removing said first dielectric layer;

forming lightly doped drain regions in said base substrate after removing said first dielectric layer, said lightly doped drain regions formed within said base substrate adjacent to said damascene gate structure and said damascene local interconnect structure;

forming spacers against the vertical walls of said damascene gate structure and said damascene local interconnect structure; and[[,]]

forming doped source/drain regions in said base substrate after forming said spacers such that said base substrate is doped more deeply into said base substrate adjacent to said spacers than into said base substrate underneath said spacers.

17-38. (canceled)

39. (currently amended) A method of fabricating a semiconductor device comprising:

forming an isolation trench in a base substrate;

forming a first dielectric layer over said base substrate;

forming a first patterned mask over said first dielectric layer;

etching through said first dielectric layer to said base substrate in areas defined by said first patterned mask to define a damascen trench in said first dielectric layer, said damascen trench having a gate area and a local interconnect area[[;]], and

positioned such that at least a portion of said damascene trench at least partially overlies said isolation trench;

stripping said first patterned mask from said first dielectric layer;

growing an oxide layer on said base substrate, said oxide layer within said gate area of said damascene trench defining a gate oxide layer;

forming a second patterned mask over said semiconductor device, said second patterned mask arranged to expose at least a portion of said oxide layer within said local interconnect area;

C2 Cont.

etching away the exposed portion of said oxide layer within said damascene trench;

providing at least one contact implant within said base substrate through said damascene trench;

stripping said second patterned mask from said semiconductor device;

depositing a conductive layer comprising a conductive material over said device such that said conductive layer fills said damascene trench;

planarizing said conductive layer down to the surface of said dielectric layer;

removing said first dielectric layer to define a damascene gate structure and a damascene local interconnect structure;

forming lightly doped drain regions in said base substrate adjacent to said damascene gate structure and said damascene local interconnect structure;

depositing a spacer layer over said device;

anisotropically etching said spacer layer such that spacers are formed over the portions of said base substrate where said lightly doped drain regions are formed; and

forming doped source/drain regions in said base substrate after forming said spacers such that said base substrate is doped more deeply into said base substrate adjacent to said spacers than into said base substrate underneath said spacers.

40-44. (cancelled)

45. (currently amended) A m thod of fabricating a semiconductor d vic according to claim [[1]]7, wherein said local interconnect area partially overlies an isolation trench formed in said base substrate.

C2 46. (currently amended) A method of fabricating a semiconductor device according to claim [[1]]7, further comprising forming a plurality of local interconnect areas in said damascene trench.

47. (currently amended) A method of fabricating a semiconductor device according to claim [[1]]7, further comprising forming a plurality of gate areas in said damascene trench.

48. (previously presented) A method of fabricating a semiconductor device according to claim 2, wherein said isolation trench comprises a shallow trench isolation structure.

49. (previously presented) A method of fabricating a semiconductor device according to claim 6, wherein said gate area and said local interconnect area of said damascene trench are both formed by said patterned mask and etching.